# CY7C1366C, CY7C1367C

# 9-Mbit (256 K × 36/512 K × 18) Pipelined DCD Sync SRAM

## Features

- Supports bus operation up to 166 MHz
- Available speed grade is 166 MHz
- Registered inputs and outputs for pipelined operation
  - Optimal for performance (double-cycle deselect)
    - Depth expansion without wait state
  - 3.3 V – 5% and + 10% core power supply ($V_{DD}$)
- 2.5 V/3.3 V I/O power supply ($V_{DDQ}$)
- Fast clock-to-output times
  - 3.5 ns (for 166 MHz device)
- Provide high performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP and non Pb-free 119-ball BGA package
- IEEE 1149.1 JTAG-compatible boundary scan
- “ZZ” sleep mode option

## Functional Description

The CY7C1366C/CY7C1367C SRAM integrates 256 K × 36 and 512 K × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE_1}$), depth-expansion chip enables ($\overline{CE_2}$ and $\overline{CE_3}$[1]), burst control inputs (ADSC, ADSP, and ADV), write enables ($\overline{BW_X}$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle.This part supports byte write operations (see Pin Definitions on page 6 and Partial Truth Table for Read/Write on page 9 for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed. This feature enables depth expansion without penalizing system performance.

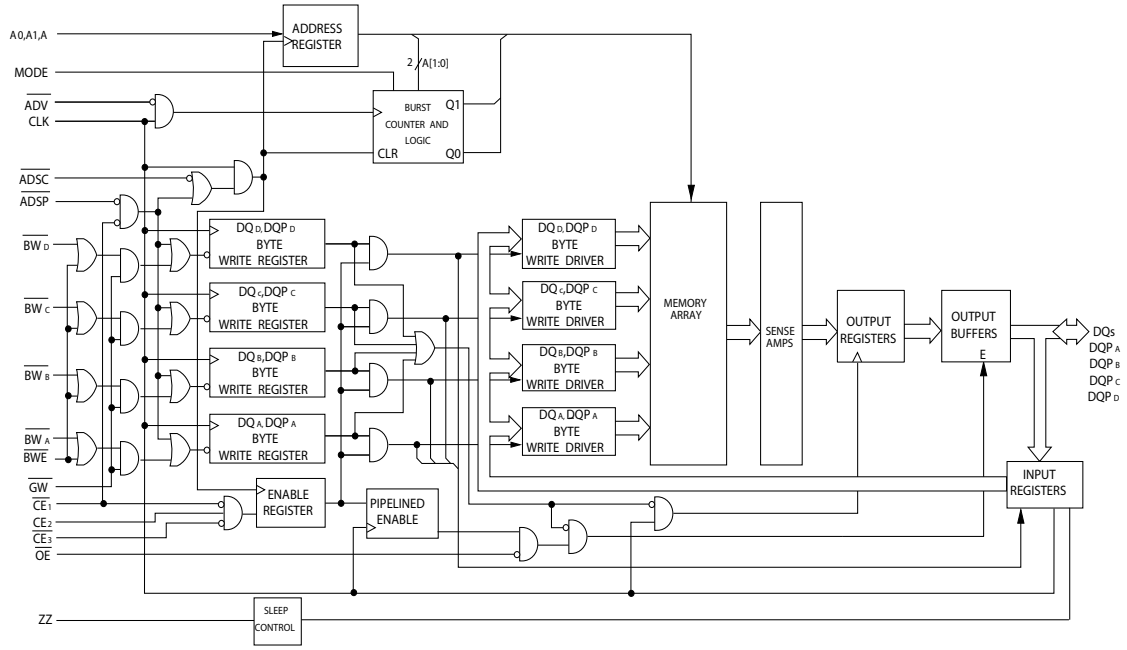
The CY7C1366C/CY7C1367C operates from a +3.3 V core power supply while all outputs operate with a +3.3 V or a +2.5 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

## Selection Guide

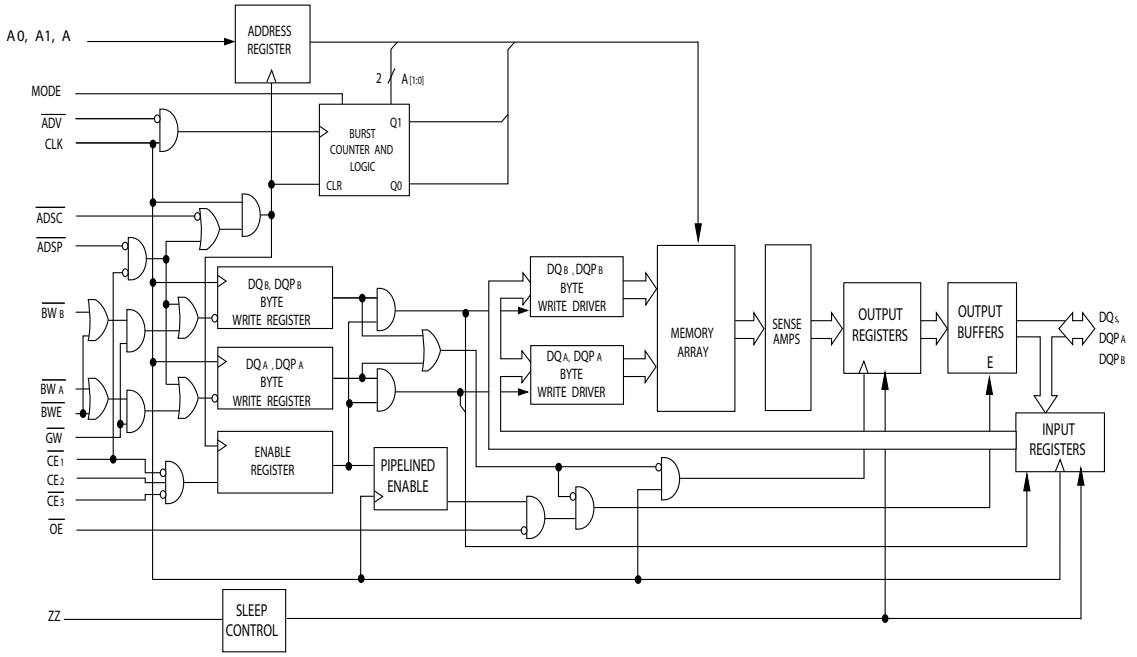
| Description | 166 MHz | Unit |
|---|---|---|
| Maximum access time | 3.5 | ns |
| Maximum operating current | 180 | mA |
| Maximum CMOS standby current | 40 | mA |

**Note**
1. $\overline{CE_3}$ is for 100-pin TQFP. 119-ball BGA is offered only in 2 Chip Enable.

## Logic Block Diagram – CY7C1366C



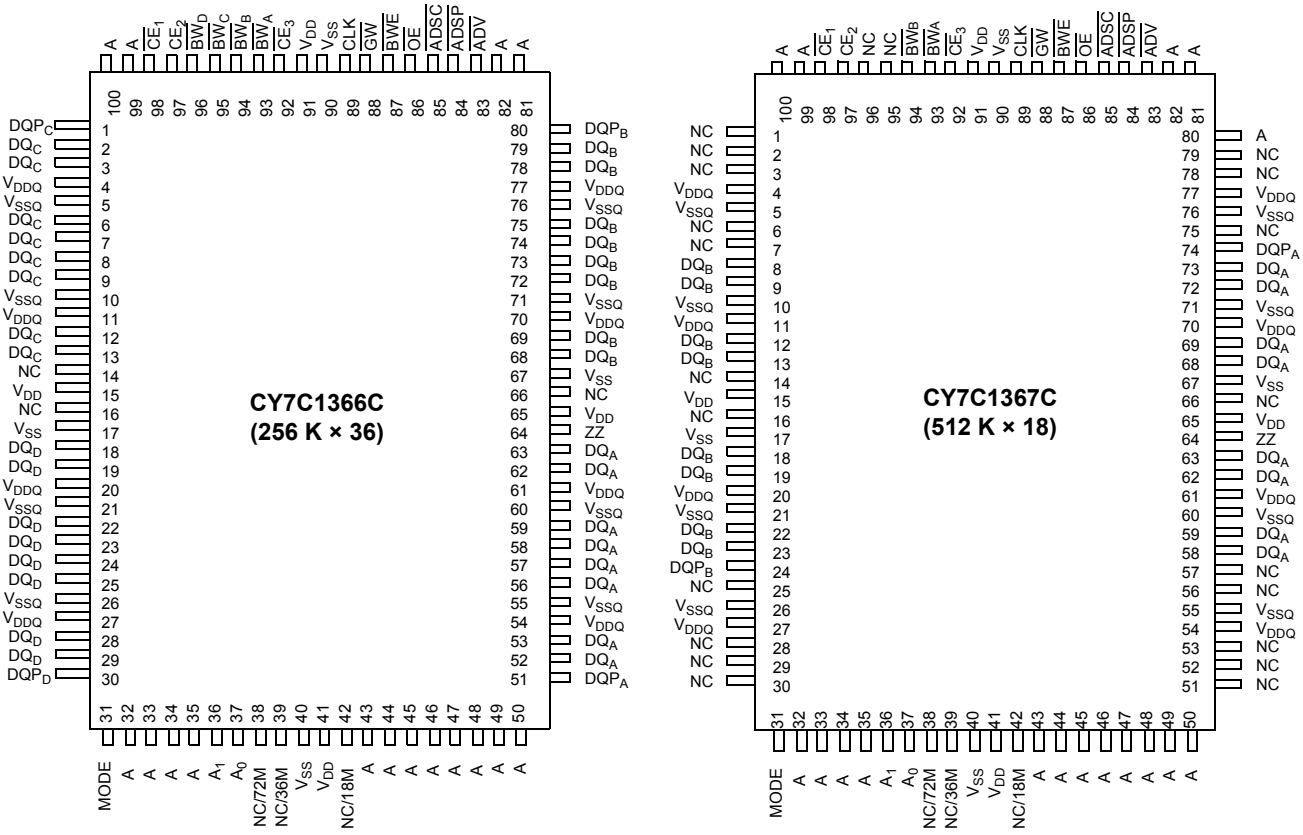

## Logic Block Diagram – CY7C1367C



## Contents

## Pin Configurations

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enables)**



## Pin Configurations *(continued)*

**Figure 2. 119-ball BGA (14 × 22 × 2.4 mm) pinout (2 Chip Enable with JTAG)**

**CY7C1366C (256 K × 36)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | $\overline{ADSP}$ | A | A | $V_{DDQ}$ |
| **B** | NC/288M | $CE_2$ | A | $\overline{ADSC}$ | A | A | NC/576M |
| **C** | NC/144M | A | A | $V_{DD}$ | A | A | NC/1G |
| **D** | $DQ_C$ | $DQP_C$ | $V_{SS}$ | NC | $V_{SS}$ | $DQP_B$ | $DQ_B$ |
| **E** | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $\overline{CE_1}$ | $V_{SS}$ | $DQ_B$ | $DQ_B$ |
| **F** | $V_{DDQ}$ | $DQ_C$ | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $DQ_B$ | $V_{DDQ}$ |
| **G** | $DQ_C$ | $DQ_C$ | $\overline{BW_C}$ | $\overline{ADV}$ | $\overline{BW_B}$ | $DQ_B$ | $DQ_B$ |
| **H** | $DQ_C$ | $DQ_C$ | $V_{SS}$ | $\overline{GW}$ | $V_{SS}$ | $DQ_B$ | $DQ_B$ |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | $DQ_D$ | $DQ_D$ | $V_{SS}$ | CLK | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| **L** | $DQ_D$ | $DQ_D$ | $\overline{BW_D}$ | NC | $\overline{BW_A}$ | $DQ_A$ | $DQ_A$ |
| **M** | $V_{DDQ}$ | $DQ_D$ | $V_{SS}$ | $\overline{BWE}$ | $V_{SS}$ | $DQ_A$ | $V_{DDQ}$ |
| **N** | $DQ_D$ | $DQ_D$ | $V_{SS}$ | A1 | $V_{SS}$ | $DQ_A$ | $DQ_A$ |
| **P** | $DQ_D$ | $DQP_D$ | $V_{SS}$ | A0 | $V_{SS}$ | $DQP_A$ | $DQ_A$ |
| **R** | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| **T** | NC | NC/72M | A | A | A | NC/36M | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

## Pin Definitions

| Name | I/O | Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-synchronous | **Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$[2] are sampled active. A1:A0 are fed to the two-bit counter. |
| $\overline{BW_A}$,$\overline{BW_B}$, $\overline{BW_C}$,$\overline{BW_D}$ | Input-synchronous | **Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK. |
| $\overline{GW}$ | Input-synchronous | **Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (All bytes are written, regardless of the values on $\overline{BW_X}$ and $\overline{BWE}$). |
| $\overline{BWE}$ | Input-synchronous | **Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write. |
| CLK | Input-clock | **Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation. |
| $\overline{CE_1}$ | Input-synchronous | **Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE_3}$[2] to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded. |
| $CE_2$ | Input-synchronous | **Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$[2] to select/deselect the device. $CE_2$ is sampled only when a new external address is loaded. |
| $\overline{CE_3}$[2] | Input-synchronous | **Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $CE_2$ to select/deselect the device. Not connected for BGA. Where referenced, $\overline{CE_3}$[2] is assumed active throughout this document for BGA.<br>$\overline{CE_3}$ is sampled only when a new external address is loaded. |
| $\overline{OE}$ | Input-asynchronous | **Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state. |
| $\overline{ADV}$ | Input-synchronous | **Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle. |
| $\overline{ADSP}$ | Input-synchronous | **Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE_1}$ is deasserted HIGH. |
| $\overline{ADSC}$ | Input-synchronous | **Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. |
| ZZ | Input-asynchronous | **ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down. |
| DQs, DQPs | I/O-synchronous | **Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and $DQP_X$ are placed in a tristate condition. |
| $V_{DD}$ | Power supply | **Power supply inputs to the core of the device**. |
| $V_{SS}$ | Ground | **Ground for the core of the device**. |
| $V_{SSQ}$ | I/O ground | **Ground for the I/O circuitry**. |
| $V_{DDQ}$ | I/O power supply | **Power supply for the I/O circuitry**. |

**Note**
2. $\overline{CE_3}$ is for 100-pin TQFP. 119-ball BGA is offered only in 2 Chip Enable.

## Pin Definitions *(continued)*

| Name | I/O | Description |
|---|---|---|
| MODE | Input-static | **Selects burst order**. When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up. |
| TDO | JTAG serial output synchronous | **Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin should be disconnected. This pin is not available on TQFP packages. |
| TDI | JTAG serial input synchronous | **Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to $V_{DD}$. This pin is not available on TQFP packages. |
| TMS | JTAG serial input synchronous | **Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to $V_{DD}$. This pin is not available on TQFP packages. |
| TCK | JTAG-clock | **Clock input to the JTAG circuitry**. If the JTAG feature is not being used, this pin must be connected to $V_{SS}$. This pin is not available on TQFP packages. |
| NC | – | **No connects**. Not internally connected to the die.18M, 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die. |

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1366C/CY7C1367C supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BWE}$) and byte write select ($\overline{BW_X}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous chip selects $\overline{CE_1}$, $CE_2$, $\overline{CE_3}$[3] and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and on the data bus within $t_{CO}$ if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported.

The CY7C1366C/CY7C1367C is a double-cycle deselect part. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will tristate immediately after the next clock rise.

**Note**
3. $\overline{CE_3}$ is for 100-pin TQFP. 119-ball BGA is offered only in 2 Chip Enable.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the $DQ_x$ inputs is written into the corresponding address location in the memory core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW_X}$ signals. The CY7C1366C/CY7C1367C provides byte write capability that is described in the Write Cycle Description table. Asserting the byte write enable input ($\overline{BWE}$) with the selected byte write input will selectively write to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism is provided to simplify the write operations.

Because the CY7C1366C/CY7C1367C is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so tristates the output drivers. As a safety precaution, DQ are automatically tristated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_X$ is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self-timed write mechanism is provided to simplify the write operations.

Because the CY7C1366C/CY7C1367C is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the $DQ_X$ inputs. Doing so tristates the output drivers. As a safety precaution, $DQ_X$ are automatically tristated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

### Burst Sequences

The CY7C1366C/CY7C1367C provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation ‘sleep’ mode. Two clock cycles are required to enter into or exit from this ‘sleep’ mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the ‘sleep’ mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the ‘sleep’ mode. $\overline{CE}$s, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or $V_{DD}$)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

### ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | $ZZ \geq V_{DD} - 0.2$ V | – | 50 | mA |
| $t_{ZZS}$ | Device operation to ZZ | $ZZ \geq V_{DD} - 0.2$ V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | $ZZ \leq 0.2$ V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

## Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1366C follows. [4, 5]

| Function (CY7C1366C) | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_D}$ | $\overline{BW_C}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write byte A – ($DQ_A$ and $DQP_A$) | H | L | H | H | H | L |
| Write byte B – ($DQ_B$ and $DQP_B$) | H | L | H | H | L | H |
| Write bytes B, A | H | L | H | H | L | L |
| Write byte C – ($DQ_C$ and $DQP_C$) | H | L | H | L | H | H |
| Write bytes C, A | H | L | H | L | H | L |
| Write bytes C, B | H | L | H | L | L | H |
| Write bytes C, B, A | H | L | H | L | L | L |
| Write byte D – ($DQ_D$ and $DQP_D$) | H | L | L | H | H | H |
| Write bytes D, A | H | L | L | H | H | L |
| Write bytes D, B | H | L | L | H | L | H |
| Write bytes D, B, A | H | L | L | H | L | L |
| Write bytes D, C | H | L | L | L | H | H |
| Write bytes D, C, A | H | L | L | L | H | L |
| Write bytes D, C, B | H | L | L | L | L | H |
| Write all bytes | H | L | L | L | L | L |
| Write all bytes | L | X | X | X | X | X |

## Partial Truth Table for Read/Write

The Partial Truth Table for Read/Write for CY7C1367C follows. [4, 5]

| Function (CY7C1367C) | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|
| Read | H | H | X | X |
| Read | H | L | H | H |
| Write byte A – ($DQ_A$ and $DQP_A$) | H | L | H | L |
| Write byte B – ($DQ_B$ and $DQP_B$) | H | L | L | H |
| Write all bytes | H | L | L | L |
| Write all bytes | L | X | X | X |

**Notes**
4. All voltages referenced to $V_{SS}$ (GND).
5. This part has a voltage regulator internally; $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1366C incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1366C contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device comes up in a reset state which does not interfere with the operation of the device.

### Test Access Port (TAP)

*Test Clock (TCK)*

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

*Test Mode Select (TMS)*

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

*Test Data-In (TDI)*

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram on page 12. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register.

*Test Data-Out (TDO)*

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Identification Codes on page 16). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

*Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 13. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board-level serial test data path.

*Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

*Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order on page 17 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

*Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 16.

## TAP Instruction Set

*Overview*

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Identification Codes on page 16. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

*EXTEST*

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a high Z state.

*IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

*SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high Z state.

*SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ($t_{CS}$ and $t_{CH}$). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

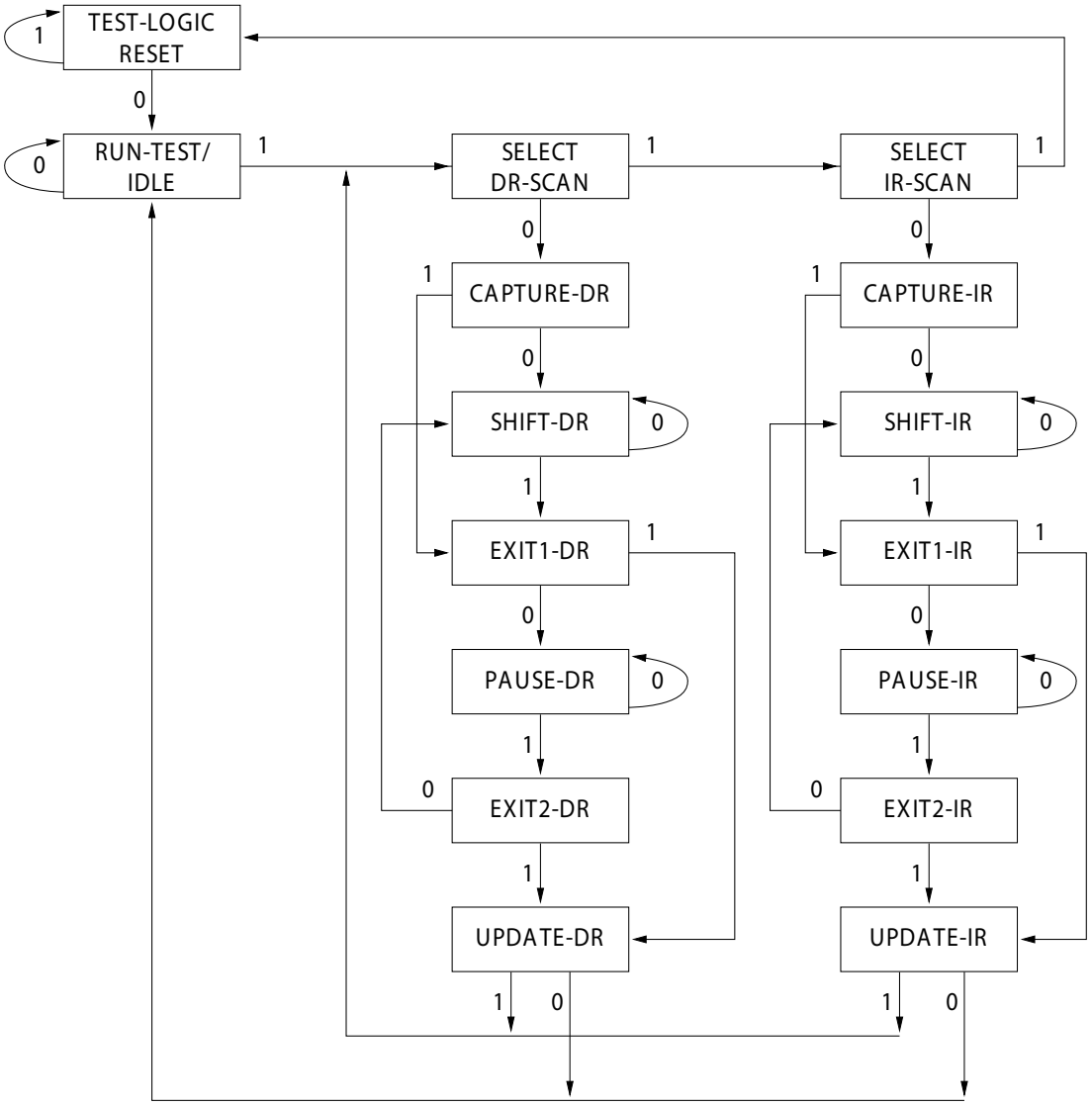
*BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

*Reserved*

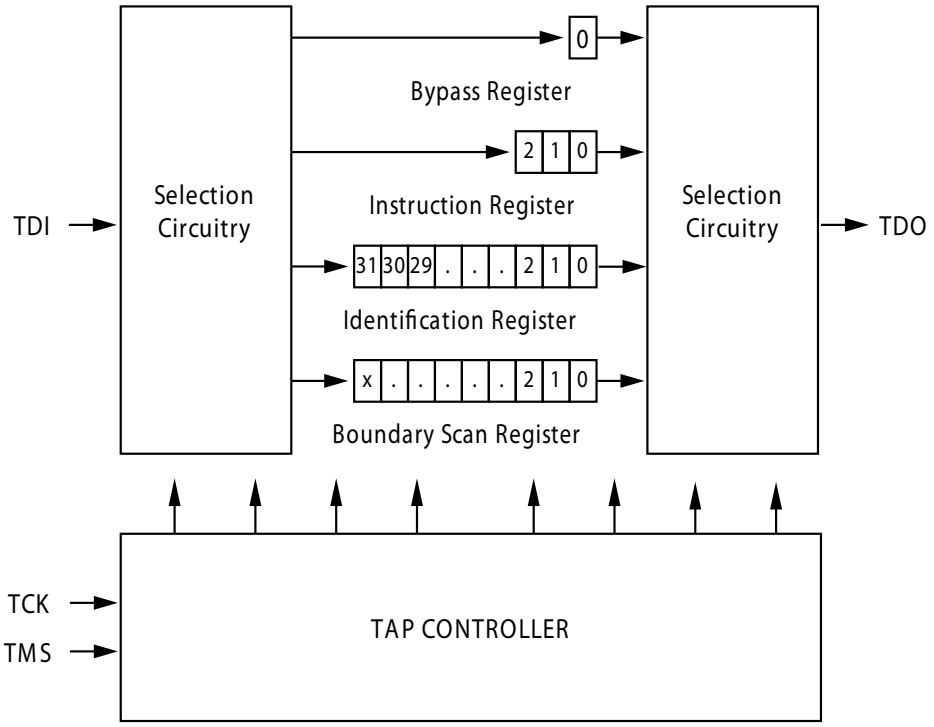
These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

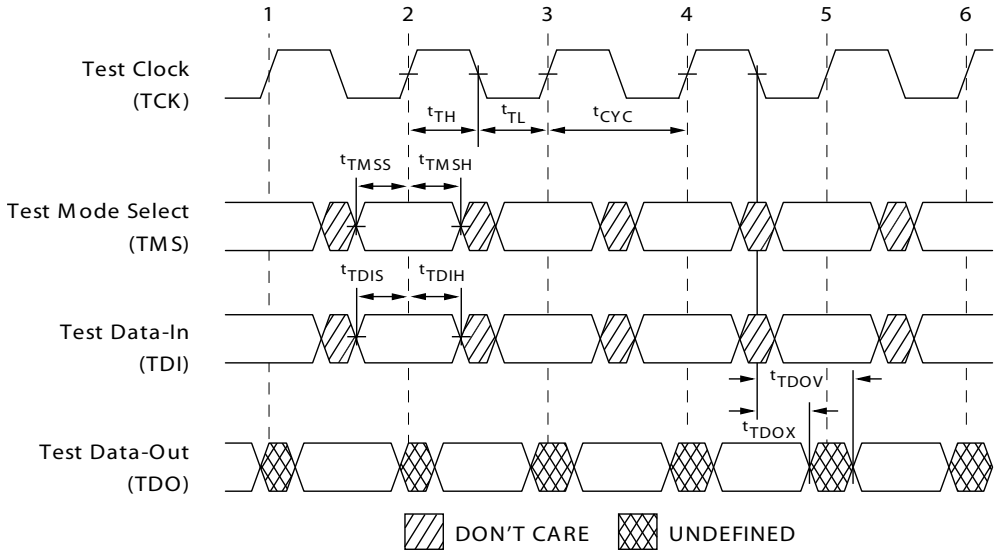



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

## TAP Controller Block Diagram




## TAP Timing



## TAP AC Switching Characteristics

Over the Operating Range

| Parameter [6, 7] | Description | Min | Max | Unit |
|---|---|---|---|---|
| **Clock** | | | | |
| $t_{TCYC}$ | TCK clock cycle time | 50 | – | ns |
| $t_{TF}$ | TCK clock frequency | – | 20 | MHz |
| $t_{TH}$ | TCK clock HIGH time | 20 | – | ns |
| $t_{TL}$ | TCK clock LOW time | 20 | – | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK clock LOW to TDO valid | – | 10 | ns |
| $t_{TDOX}$ | TCK clock LOW to TDO invalid | 0 | – | ns |
| **Setup Times** | | | | |
| $t_{TMSS}$ | TMS setup to TCK clock rise | 5 | – | ns |
| $t_{TDIS}$ | TDI setup to TCK clock rise | 5 | – | ns |
| $t_{CS}$ | Capture setup to TCK rise | 5 | – | ns |
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS hold after TCK clock rise | 5 | – | ns |
| $t_{TDIH}$ | TDI hold after clock rise | 5 | – | ns |
| $t_{CH}$ | Capture hold after clock rise | 5 | – | ns |

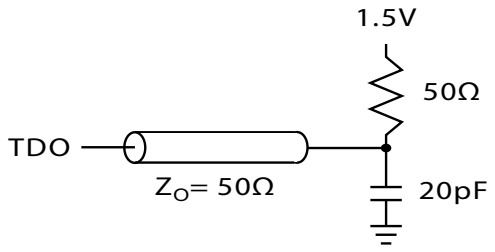
### 3.3 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 3.3 V
Input rise and fall times..... 1 ns
Input timing reference levels..... 1.5 V
Output reference levels ..... 1.5 V
Test load termination supply voltage ..... 1.5 V

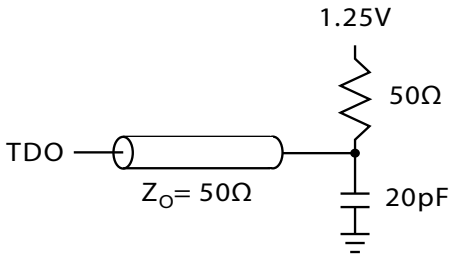
### 2.5 V TAP AC Test Conditions

Input pulse levels ..... $V_{SS}$ to 2.5 V
Input rise and fall time ..... 1 ns
Input timing reference levels..... 1.25 V
Output reference levels ..... 1.25 V
Test load termination supply voltage ..... 1.25 V

### 3.3 V TAP AC Output Load Equivalent




### 2.5 V TAP AC Output Load Equivalent




**Notes**
6. $t_{CS}$ and $t_{CH}$ refer to the setup and hold time requirements of latching data from the boundary scan register.
7. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F$ = 1 ns.

## TAP DC Electrical Characteristics and Operating Conditions

(0 °C < $T_A$ < +70 °C; $V_{DD}$ = 3.3 V ± 0.165 V unless otherwise noted)

| Parameter [8] | Description | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH voltage | $I_{OH}$ = –4.0 mA | $V_{DDQ}$ = 3.3 V | 2.4 | – | V |
| | | $I_{OH}$ = –1.0 mA | $V_{DDQ}$ = 2.5 V | 2.0 | – | V |
| $V_{OH2}$ | Output HIGH voltage | $I_{OH}$ = –100 µA | $V_{DDQ}$ = 3.3 V | 2.9 | – | V |
| | | | $V_{DDQ}$ = 2.5 V | 2.1 | – | V |
| $V_{OL1}$ | Output LOW voltage | $I_{OL}$ = 8.0 mA | $V_{DDQ}$ = 3.3 V | – | 0.4 | V |
| | | $I_{OL}$ = 8.0 mA | $V_{DDQ}$ = 2.5 V | – | 0.4 | V |
| $V_{OL2}$ | Output LOW voltage | $I_{OL}$ = 100 µA | $V_{DDQ}$ = 3.3 V | – | 0.2 | V |
| | | | $V_{DDQ}$ = 2.5 V | – | 0.2 | V |
| $V_{IH}$ | Input HIGH voltage | | $V_{DDQ}$ = 3.3 V | 2.0 | $V_{DD}$ + 0.3 | V |
| | | | $V_{DDQ}$ = 2.5 V | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | | $V_{DDQ}$ = 3.3 V | –0.5 | 0.7 | V |
| | | | $V_{DDQ}$ = 2.5 V | –0.3 | 0.7 | V |
| $I_X$ | Input load current | GND ≤ $V_{IN}$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |

**Notes**
8. All voltages referenced to $V_{SS}$ (GND).

## Identification Register Definitions

| Instruction Field | CY7C1366C (256 K × 36) | Description |
|---|---|---|
| Revision number (31:29) | 000 | Describes the version number. |
| Device depth (28:24) [9] | 01011 | Reserved for Internal Use |
| Device width (23:18) 119-ball BGA | 101110 | Defines memory type and architecture |
| Cypress device ID (17:12) | 100110 | Defines width and density |
| Cypress JEDEC ID code (11:1) | 00000110100 | Allows unique identification of SRAM vendor. |
| ID register presence indicator (0) | 1 | Indicates the presence of an ID register. |

## Scan Register Sizes

| Register Name | Bit Size (× 36) |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary scan order (119-ball BGA package) | 71 |

## Identification Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations. |
| SAMPLE Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operations. |

**Note**
9. Bit #24 is “1” in the Register Definitions for both 2.5 V and 3.3 V versions of this device.

## Boundary Scan Order

119-ball BGA

**CY7C1366C (256 K × 36)**

| Bit # | Ball ID | Signal Name |
|---|---|---|
| 1 | K4 | CLK |
| 2 | H4 | $\overline{GW}$ |
| 3 | M4 | $\overline{BWE}$ |
| 4 | F4 | $\overline{OE}$ |
| 5 | B4 | $\overline{ADSC}$ |
| 6 | A4 | $\overline{ADSP}$ |
| 7 | G4 | $\overline{ADV}$ |
| 8 | C3 | A |
| 9 | B3 | A |
| 10 | D6 | $DQP_B$ |
| 11 | H7 | $DQ_B$ |
| 12 | G6 | $DQ_B$ |
| 13 | E6 | $DQ_B$ |
| 14 | D7 | $DQ_B$ |
| 15 | E7 | $DQ_B$ |
| 16 | F6 | $DQ_B$ |
| 17 | G7 | $DQ_B$ |
| 18 | H6 | $DQ_B$ |
| 19 | T7 | ZZ |
| 20 | K7 | $DQ_A$ |
| 21 | L6 | $DQ_A$ |
| 22 | N6 | $DQ_A$ |
| 23 | P7 | $DQ_A$ |
| 24 | N7 | $DQ_A$ |
| 25 | M6 | $DQ_A$ |
| 26 | L7 | $DQ_A$ |
| 27 | K6 | $DQ_A$ |
| 28 | P6 | $DQP_A$ |
| 29 | T4 | A |
| 30 | A3 | A |
| 31 | C5 | A |
| 32 | B5 | A |
| 33 | A5 | A |
| 34 | C6 | A |
| 35 | A6 | A |
| 36 | B6 | A |

| Bit # | Ball ID | Signal Name |
|---|---|---|
| 37 | P4 | A0 |
| 38 | N4 | A1 |
| 39 | R6 | A |
| 40 | T5 | A |
| 41 | T3 | A |
| 42 | R2 | A |
| 43 | R3 | MODE |
| 44 | P2 | $DQP_D$ |
| 45 | P1 | $DQ_D$ |
| 46 | L2 | $DQ_D$ |
| 47 | K1 | $DQ_D$ |
| 48 | N2 | $DQ_D$ |
| 49 | N1 | $DQ_D$ |
| 50 | M2 | $DQ_D$ |
| 51 | L1 | $DQ_D$ |
| 52 | K2 | $DQ_D$ |
| 53 | Internal | Internal |
| 54 | H1 | $DQ_C$ |
| 55 | G2 | $DQ_C$ |
| 56 | E2 | $DQ_C$ |
| 57 | D1 | $DQ_C$ |
| 58 | H2 | $DQ_C$ |
| 59 | G1 | $DQ_C$ |
| 60 | F2 | $DQ_C$ |
| 61 | E1 | $DQ_C$ |
| 62 | D2 | $DQP_C$ |
| 63 | C2 | A |
| 64 | A2 | A |
| 65 | E4 | $\overline{CE_1}$ |
| 66 | B2 | $CE_2$ |
| 67 | L3 | $\overline{BWD}$ |
| 68 | G3 | $\overline{BW_C}$ |
| 69 | G5 | $\overline{BW_B}$ |
| 70 | L5 | $\overline{BW_A}$ |
| 71 | Internal | Internal |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{DD}$ relative to GND .....–0.5 V to +4.6 V

Supply voltage on $V_{DDQ}$ relative to GND ..... –0.5 V to +$V_{DD}$

DC voltage applied to outputs in tristate .....–0.5 V to $V_{DDQ}$ + 0.5 V

DC input voltage .....–0.5 V to $V_{DD}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .....> 2001 V

Latch-up current .....> 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to $V_{DD}$ |

## Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|---|---|---|---|---|---|
| LSBU | Logical single-bit upsets | 25 °C | 361 | 394 | FIT/ Mb |
| LMBU | Logical multi-bit upsets | 25 °C | 0 | 0.01 | FIT/ Mb |
| SEL | Single event latch-up | 85 °C | 0 | 0.1 | FIT/ Dev |

** No LMBU or SEL events occurred during testing*; this column represents a statistical $\chi^2$, 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

## Electrical Characteristics

Over the Operating Range

| Parameter [10, 11] | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | I/O supply voltage | for 3.3 V I/O | 3.135 | $V_{DD}$ | V |
| | | for 2.5 V I/O | 2.375 | 2.625 | V |
| $V_{OH}$ | Output HIGH voltage | for 3.3 V I/O, $I_{OH}$ = –4.0 mA | 2.4 | – | V |
| | | for 2.5 V I/O, $I_{OH}$ = –1.0 mA | 2.0 | – | V |
| $V_{OL}$ | Output LOW voltage | for 3.3 V I/O, $I_{OL}$= 8.0 mA | – | 0.4 | V |
| | | for 2.5 V I/O, $I_{OL}$= 1.0 mA | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage [10] | for 3.3 V I/O | 2.0 | $V_{DD}$ + 0.3 | V |
| | | for 2.5 V I/O | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage [10] | for 3.3 V I/O | –0.3 | 0.8 | V |
| | | for 2.5 V I/O | –0.3 | 0.7 | V |
| $I_X$ | Input leakage current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | –5 | 5 | µA |
| | Input current of MODE | Input = $V_{SS}$ | –30 | – | µA |
| | | Input = $V_{DD}$ | – | 5 | µA |
| | Input current of ZZ | Input = $V_{SS}$ | –5 | – | µA |
| | | Input = $V_{DD}$ | – | 30 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_I$ ≤ $V_{DDQ}$, output disabled | –5 | 5 | µA |

**Notes**
10. Overshoot: $V_{IH(AC)} < V_{DD} + 1.5$ V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)} > -2$ V (Pulse width less than $t_{CYC}/2$).
11. $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

## Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter [10, 11] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | $V_{DD}$ operating supply current | $V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 6 ns cycle, 166 MHz | – | 180 | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | $V_{DD}$ = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = $f_{MAX}$ = $1/t_{CYC}$ | 6 ns cycle, 166 MHz | – | 110 | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | $V_{DD}$ = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0 | 6 ns cycle, 166 MHz | – | 40 | mA |
| $I_{SB3}$ | Automatic CE power-down current – CMOS inputs | $V_{DD}$ = Max, device deselected, or $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V f = $f_{MAX}$ = $1/t_{CYC}$ | 6 ns cycle, 166 MHz | – | 100 | mA |
| $I_{SB4}$ | Automatic CE power-down current – TTL inputs | $V_{DD}$ = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0 | 6 ns cycle, 166 MHz | – | 40 | mA |

## Capacitance

| Parameter [12] | Description | Test Conditions | 100-pin TQFP Max | 119-ball BGA Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 3.3 V, $V_{DDQ}$ = 2.5 V | 5 | 5 | pF |
| $C_{CLK}$ | Clock input capacitance | | 5 | 5 | pF |
| $C_{I/O}$ | Input/output capacitance | | 5 | 7 | pF |

## Thermal Resistance

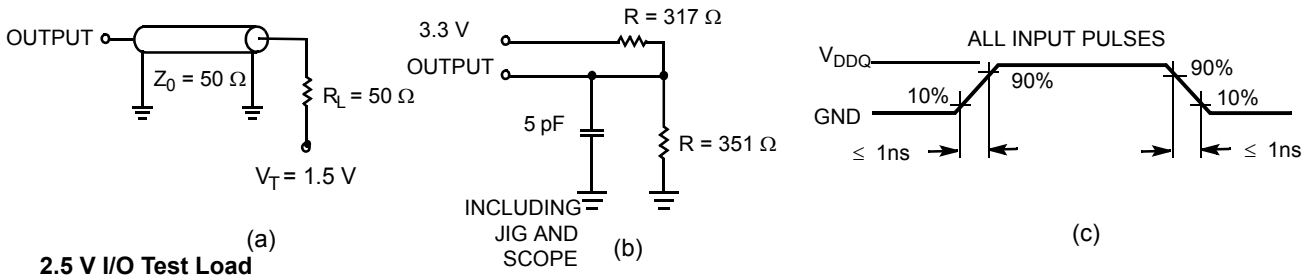
| Parameter [12] | Description | Test Conditions | 100-pin TQFP Package | 119-ball BGA Package | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 29.41 | 34.1 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 6.31 | 14.0 | °C/W |

**Note**
12. Tested initially and after any design or process change that may affect these parameters

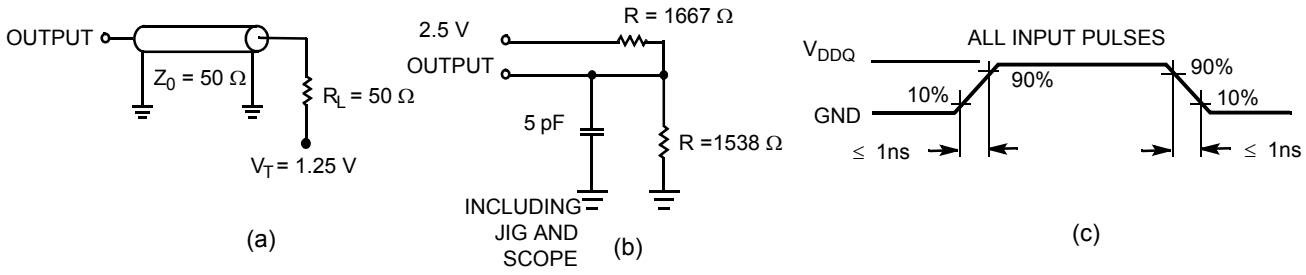
## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**

**3.3 V I/O Test Load**




**2.5 V I/O Test Load**



## Switching Characteristics

Over the Operating Range

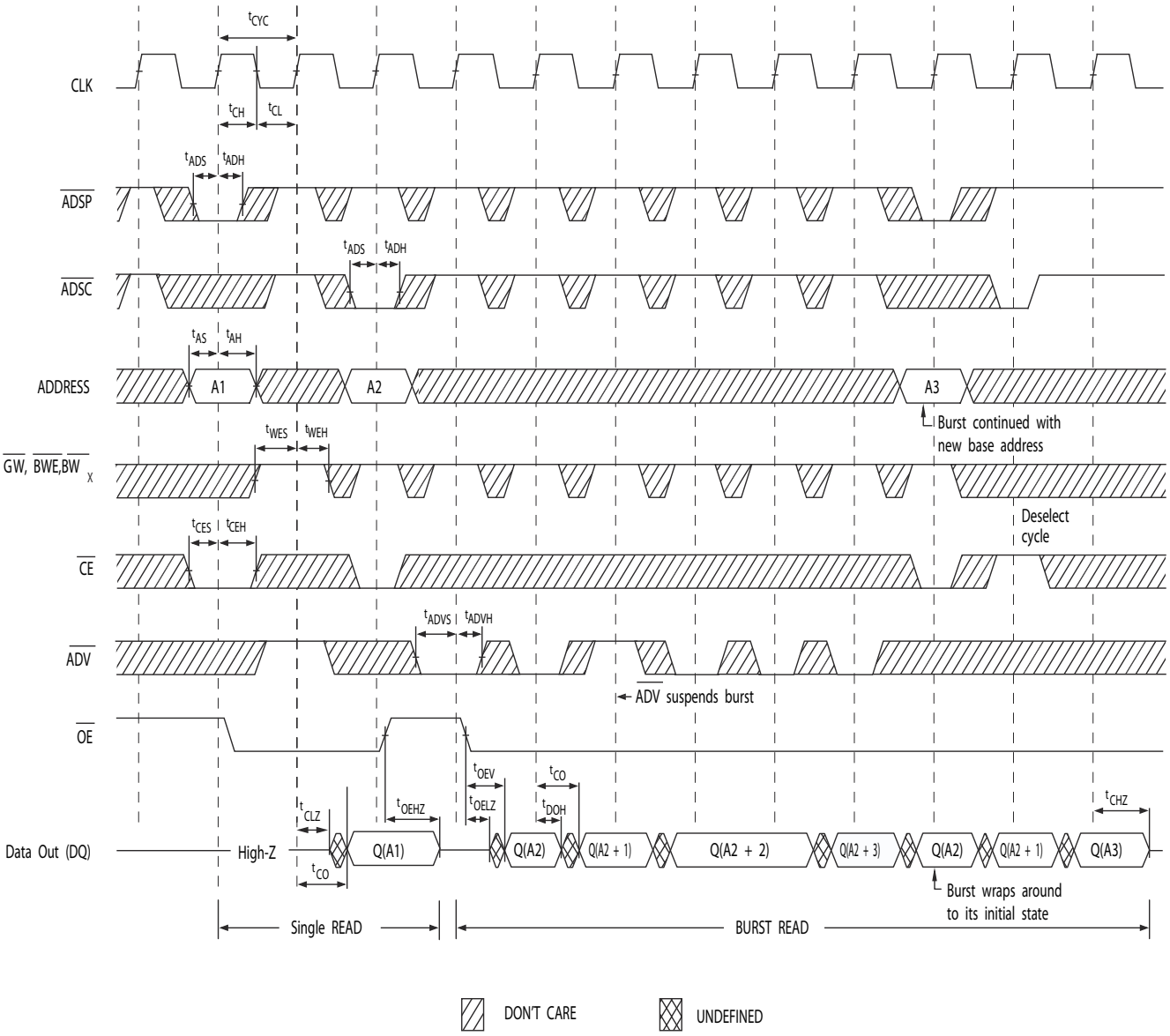
| Parameter [13, 14] | Description | -166 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{POWER}$ | $V_{DD}$(typical) to the first access [15] | 1 | – | ms |
| **Clock** | | | | |
| $t_{CYC}$ | Clock cycle time | 6.0 | – | ns |
| $t_{CH}$ | Clock HIGH | 2.4 | – | ns |
| $t_{CL}$ | Clock LOW | 2.4 | – | ns |
| **Output Times** | | | | |
| $t_{CO}$ | Data output valid after CLK rise | – | 3.5 | ns |
| $t_{DOH}$ | Data output hold after CLK rise | 1.25 | – | ns |
| $t_{CLZ}$ | Clock to low Z [16, 17, 18] | 1.25 | – | ns |
| $t_{CHZ}$ | Clock to high Z [16, 17, 18] | 1.25 | 3.5 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to output valid | – | 3.5 | ns |
| $t_{OELZ}$ | $\overline{OE}$ LOW to output low Z [16, 17, 18] | 0 | – | ns |
| $t_{OEHZ}$ | $\overline{OE}$ HIGH to output high Z [16, 17, 18] | – | 3.5 | ns |
| **Setup Times** | | | | |
| $t_{AS}$ | Address setup before CLK rise | 1.5 | – | ns |
| $t_{ADS}$ | $\overline{ADSC}$, $\overline{ADSP}$ setup before CLK rise | 1.5 | – | ns |
| $t_{ADVS}$ | $\overline{ADV}$ setup before CLK rise | 1.5 | – | ns |
| $t_{WES}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ setup before CLK rise | 1.5 | – | ns |
| $t_{DS}$ | Data input setup before CLK rise | 1.5 | – | ns |
| $t_{CES}$ | Chip enable setup before CLK rise | 1.5 | – | ns |
| **Hold Times** | | | | |
| $t_{AH}$ | Address hold after CLK rise | 0.5 | – | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise | 0.5 | – | ns |
| $t_{ADVH}$ | $\overline{ADV}$ hold after CLK rise | 0.5 | – | ns |
| $t_{WEH}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise | 0.5 | – | ns |
| $t_{DH}$ | Data input hold after CLK rise | 0.5 | – | ns |
| $t_{CEH}$ | Chip enable hold after CLK rise | 0.5 | – | ns |

**Notes**

13. Timing reference level is 1.5 V when $V_{DDQ}$ = 3.3 V and is 1.25 V when $V_{DDQ}$ = 2.5 V.
14. Test conditions shown in (a) of Figure 3 on page 20 unless otherwise noted.
15. This part has a voltage regulator internally; $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
16. $t_{CHZ}$, $t_{CLZ}$,$t_{OELZ}$, and $t_{OEHZ}$ are specified with AC test conditions shown in part (b) of Figure 3 on page 20. Transition is measured ±200 mV from steady-state voltage.
17. At any given voltage and temperature, $t_{OEHZ}$ is less than $t_{OELZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

## Switching Waveforms

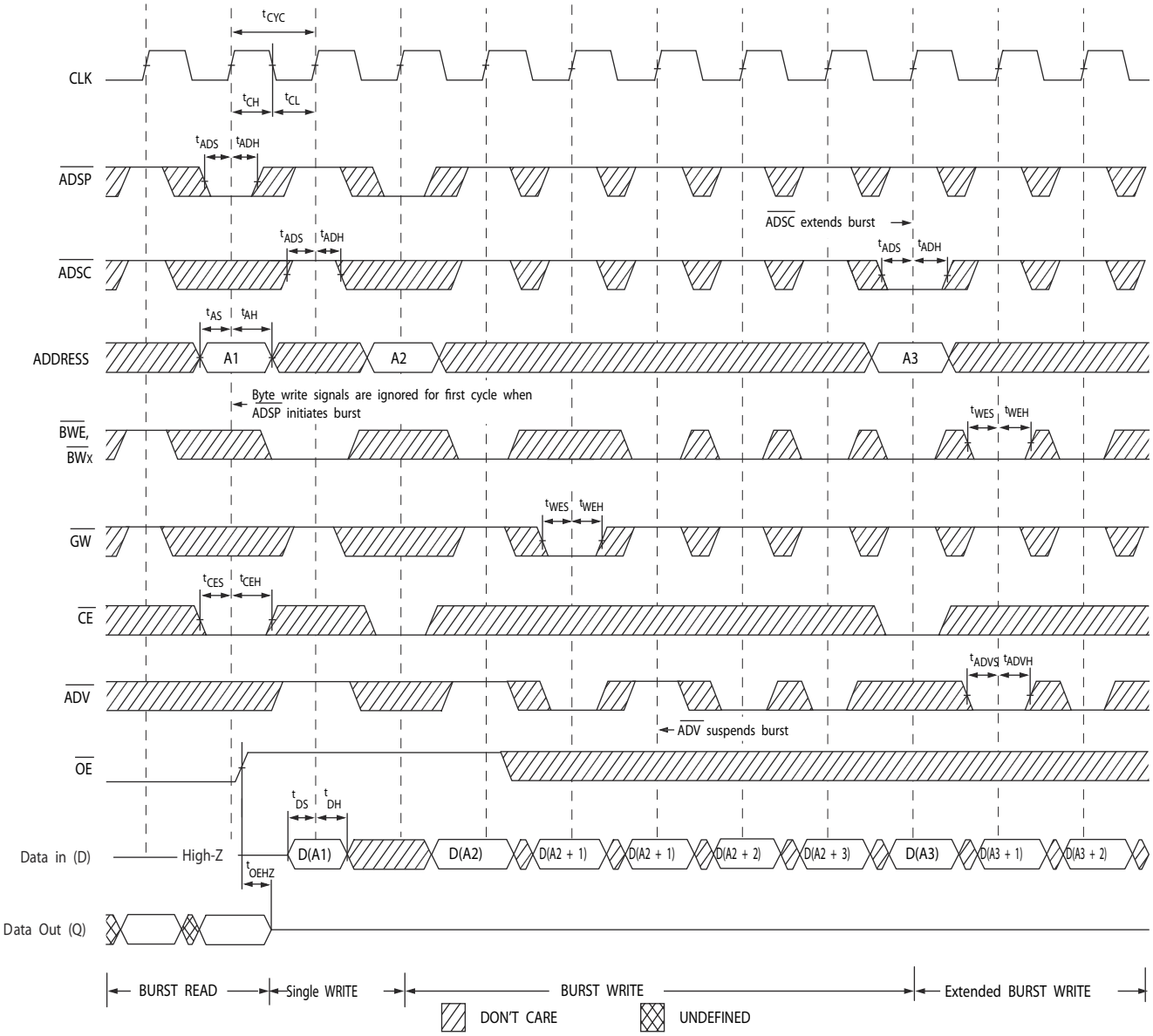
**Figure 4. Read Cycle Timing** [19]




**Note**
19. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.

## Switching Waveforms *(continued)*

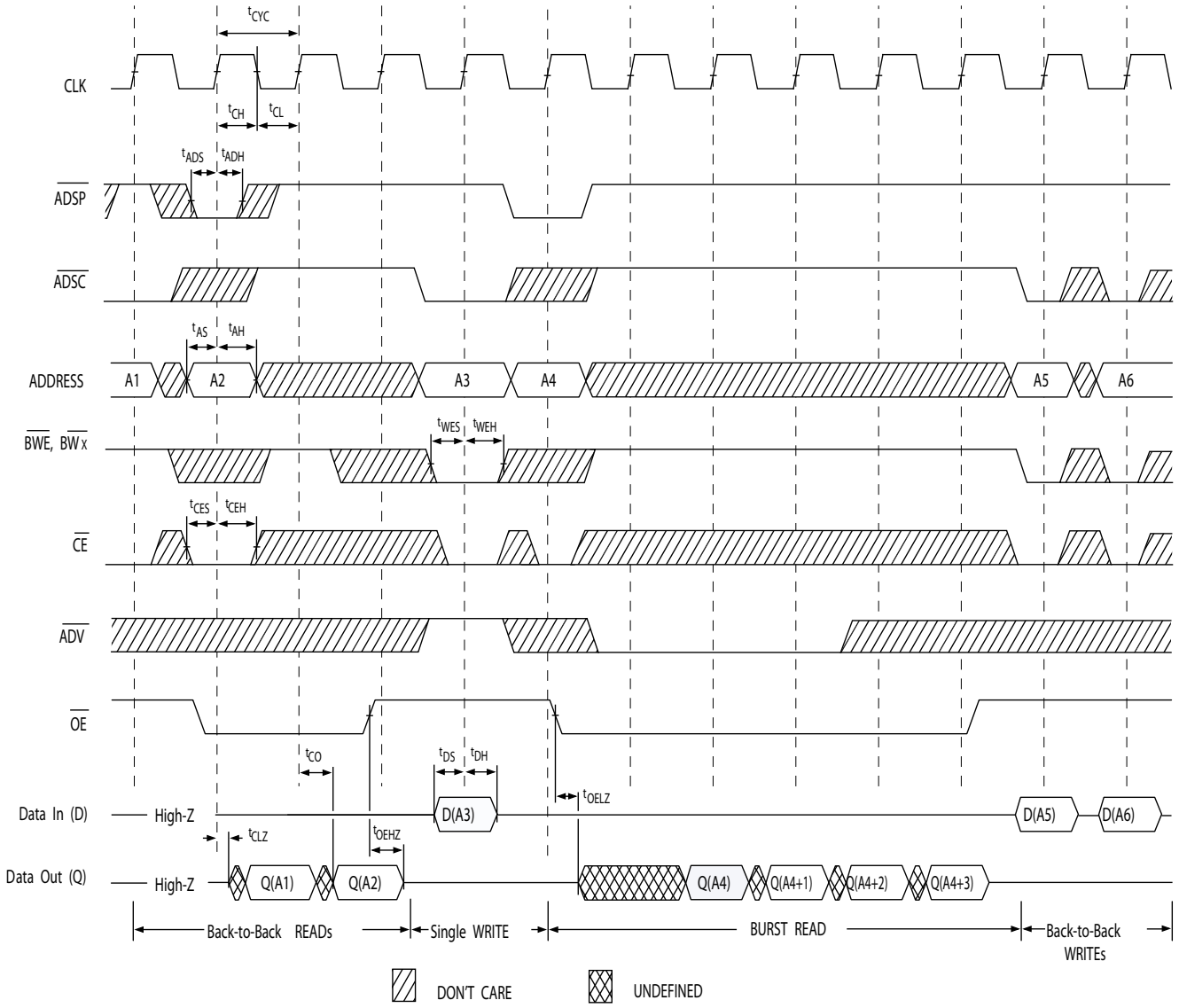
**Figure 5. Write Cycle Timing** [20, 21]




**Notes**
20. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
21. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

## Switching Waveforms *(continued)*

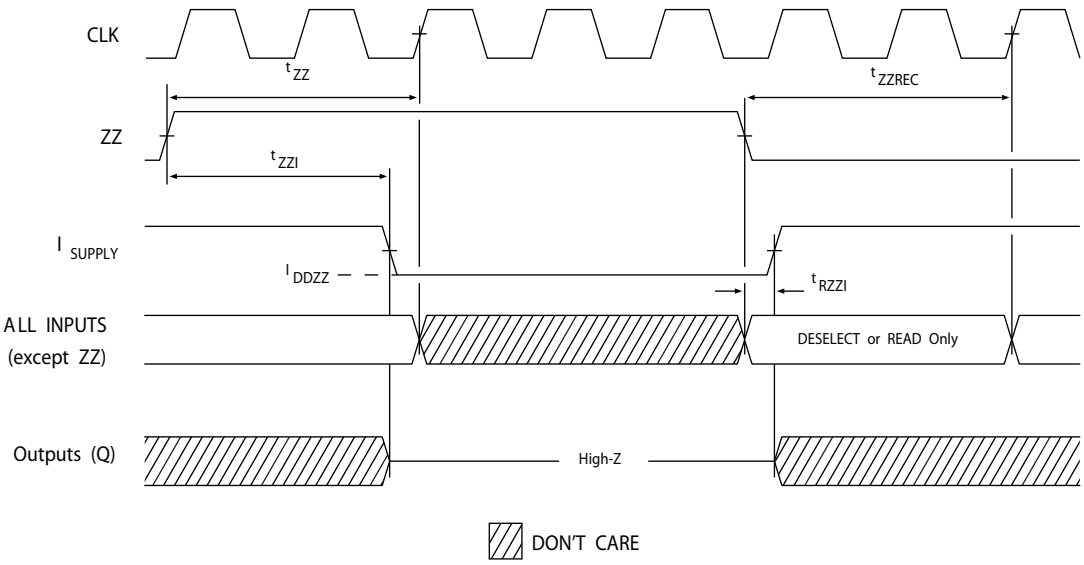
**Figure 6. Read/Write Cycle Timing** [22, 23, 24]




**Notes**
22. In this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
23. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
24. $\overline{GW}$ is HIGH.

## Switching Waveforms *(continued)*

**Figure 7. ZZ Mode Timing** [25, 26]




**Notes**
25. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
26. DQs are in high Z when exiting ZZ sleep mode.

## Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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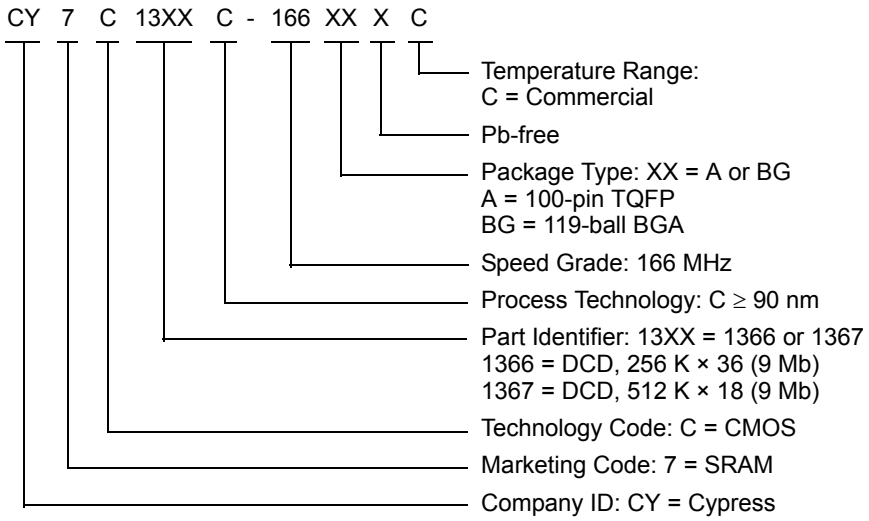
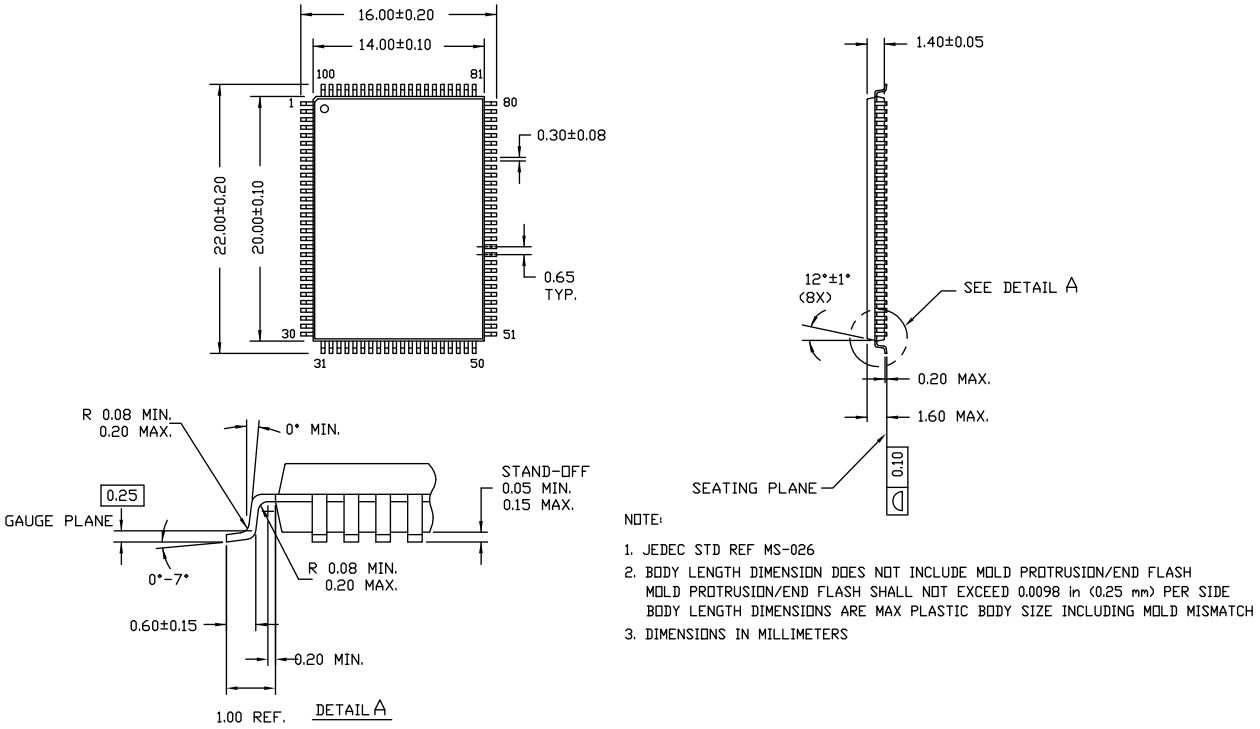
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 166 | CY7C1366C-166AXC | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Commercial |
| | CY7C1367C-166AXC | | | |
| | CY7C1366C-166BGC | 51-85115 | 119-ball BGA (14 × 22 × 2.4 mm) | |

### Ordering Code Definitions



## Package Diagrams

**Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050**



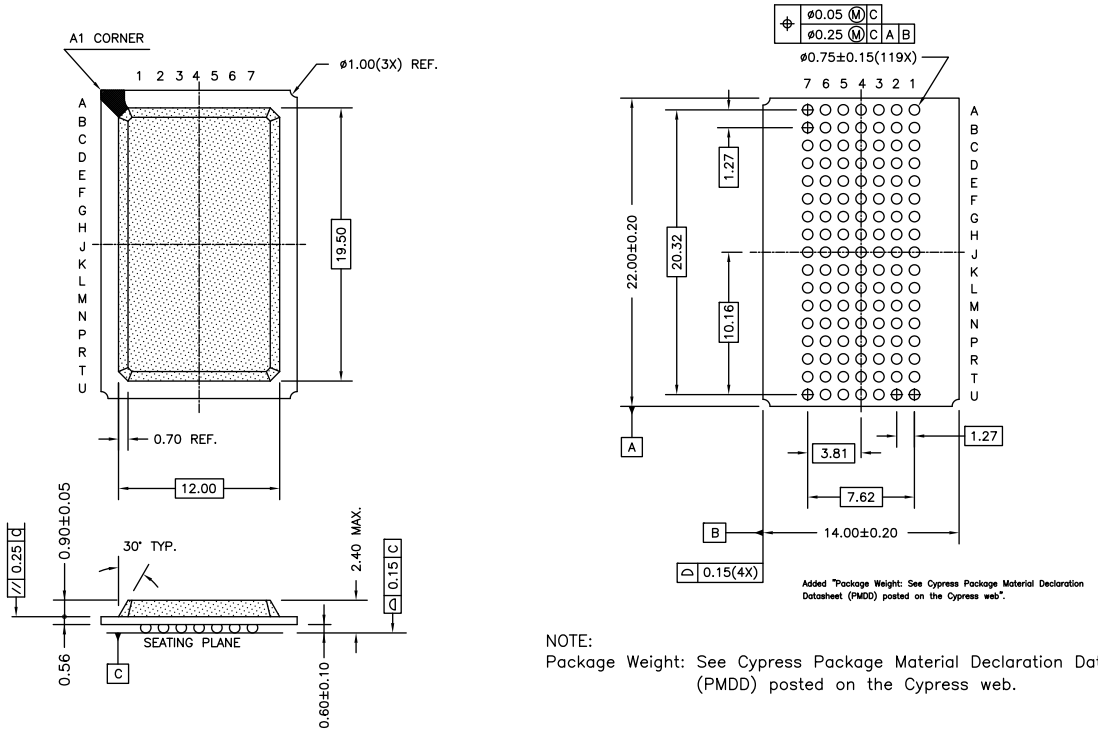

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *D

## Package Diagrams *(continued)*

**Figure 9. 119-ball PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115**




NOTE:
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 *D

## Acronyms

| Acronym | Description |
|---|---|
| BGA | ball grid array |
| $\overline{CE}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| EIA | electronic industries alliance |
| FBGA | fine-pitch ball grid array |
| I/O | input/output |
| JEDEC | joint electron devices engineering council |
| JTAG | joint test action group |
| LMBU | logical multi-bit upsets |
| LSB | least significant bit |
| LSBU | logical single-bit upsets |
| MSB | most significant bit |
| $\overline{OE}$ | output enable |
| SEL | single event latch up |
| SRAM | static random access memory |
| TAP | test access port |
| TCK | test clock |
| TMS | test mode select |
| TDI | test data-in |
| TDO | test data-out |
| TQFP | thin quad flat pack |
| TTL | transistor-transistor logic |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| nm | nanometer |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1366C/CY7C1367C, 9-Mbit (256 K × 36/512 K × 18) Pipelined DCD Sync SRAM<br>Document Number: 38-05542 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 241690 | See ECN | RKF | New data sheet. |
| *A | 278969 | See ECN | RKF | Updated Boundary Scan Order (Changed to match the B rev of these devices).<br>Updated Boundary Scan order (Changed to match the B rev of these devices). |
| *B | 332059 | See ECN | PCI | Updated Features (Changed frequency from 225 MHz to 250 MHz).<br>Updated Selection Guide (Changed frequency from 225 MHz to 250 MHz, unshaded 200 MHz and 166 MHz frequency related information).<br>Updated Pin Configurations (Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard).<br>Updated Pin Definitions (Added Address Expansion pins).<br>Updated Functional Overview (Added ZZ Mode Electrical Characteristics).<br>Updated Identification Register Definitions (Splitted Device Width (23:18) into two rows, retained the same values for 165-ball FBGA, Changed Device Width (23:18) for 119-ball BGA from 000110 to 101110).<br>Updated Electrical Characteristics (Changed frequency from 225 MHz to 250 MHz, unshaded 200 MHz and 166 MHz frequency related information, Updated Test Conditions of $V_{OL}$, $V_{OH}$ parameters, changed maximum value of $I_{SB1}$ parameter from 50 mA to 130 mA, 120 mA, and 110 mA for 250 MHz, 200 MHz, and 166 MHz, changed maximum value of $I_{SB3}$ parameter from 50 mA to 120 mA, 110 mA, and 100 mA for 250 MHz, 200 MHz, and 166 MHz).<br>Updated Thermal Resistance (Changed value of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from 25 °C/W and 9 °C/W to 29.41 °C/W and 6.31 °C/W respectively for 100-pin TQFP Package, changed value of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from 25 °C/W and 6 °C/W to 34.1 °C/W and 14.0 °C/W respectively for 119-ball BGA Package, changed value of $\Theta_{JA}$ and $\Theta_{JC}$ parameters from 27 °C/W and 6 °C/W to 16.8 °C/W and 3.0 °C/W respectively for 165-ball FBGA Package).<br>Updated Switching Characteristics (Changed frequency from 225 MHz to 250 MHz, unshaded 200 MHz and 166 MHz frequency related information, replaced minimum value of $t_{CYC}$ parameter from 4.4 ns to 4.0 ns for 250 MHz frequency).<br>Updated Ordering Information (Updated part numbers (Added lead-free information for 100-pin TQFP, 119-ball BGA and 165-ball FBGA packages)). |
| *C | 377095 | See ECN | PCI | Updated Electrical Characteristics (Updated Note 11 (Modified Test Condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$), changed maximum value of $I_{SB2}$ parameter from 30 mA to 40 mA). |
| *D | 408298 | See ECN | RXU | Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”.<br>Changed status from Preliminary to Final.<br>Updated Electrical Characteristics (Changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE” in the description of $I_X$ parameter).<br>Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). |
| *E | 501793 | See ECN | VKN | Updated TAP AC Switching Characteristics (Changed minimum value of $t_{TH}$ and $t_{TL}$ parameters from 25 ns to 20 ns, changed maximum value of $t_{TDOV}$ parameter from 5 ns to 10 ns).<br>Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND).<br>Updated Ordering Information (Updated part numbers). |
| *F | 2756940 | 08/27/2009 | VKN | Added Neutron Soft Error Immunity.<br>Updated Ordering Information (By including parts that are available, and modified the disclaimer for the Ordering information). |

## Document History Page *(continued)*

| Document Title: CY7C1366C/CY7C1367C, 9-Mbit (256 K × 36/512 K × 18) Pipelined DCD Sync SRAM<br>Document Number: 38-05542 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *G | 3046851 | 10/04/2010 | NJY | Added Ordering Code Definitions.<br>Updated Package Diagrams.<br>Added Acronyms and Units of Measure.<br>Minor edits and updated in new template. |
| *H | 3370121 | 09/13/2011 | PRIT | Updated Package Diagrams. |
| *I | 3613540 | 05/10/2012 | PRIT | Updated Features (Removed 250 MHz, 200 MHz frequencies related information, removed 165-ball FBGA Package related information).<br>Updated Functional Description (Removed the Note “For best-practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.” and its reference).<br>Updated Selection Guide (Removed 250 MHz, 200 MHz frequencies related information).<br>Updated Pin Configurations (Updated Figure 2 (Removed CY7C1367C related information), removed 165-ball FBGA Package related information).<br>Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1367C related information).<br>Updated Identification Register Definitions (Removed CY7C1367C related information).<br>Updated Scan Register Sizes (Removed “Bit Size (× 18)” column).<br>Updated Boundary Scan Order (Removed CY7C1367C related information).<br>Removed Boundary Scan Order (Corresponding to 165-ball FBGA Package).<br>Updated Operating Range (Removed Industrial Temperature Range).<br>Updated Electrical Characteristics (Removed 250 MHz, 200 MHz frequencies related information).<br>Updated Capacitance (Removed 165-ball FBGA Package related information).<br>Updated Thermal Resistance (Removed 165-ball FBGA Package related information).<br>Updated Switching Characteristics (Removed 250 MHz, 200 MHz frequencies related information).<br>Updated Package Diagrams (Removed 165-ball FBGA Package related information (spec 51-85180)). |
| *J | 3755966 | 09/26/2012 | PRIT | Updated Package Diagrams (spec 51-85115 (Changed revision from *C to *D)). |

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